20/6/25 AN

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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

ADDITIONAL CONTROLLER OF EXAMINATIONS AU CHENNAI 600 025

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, APR / MAY 2025

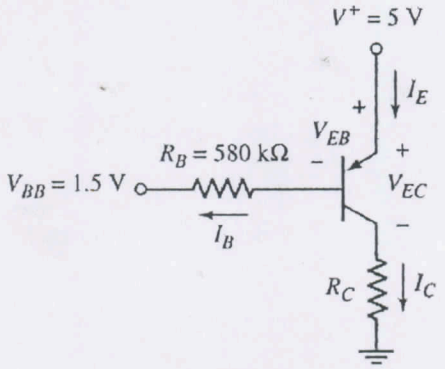
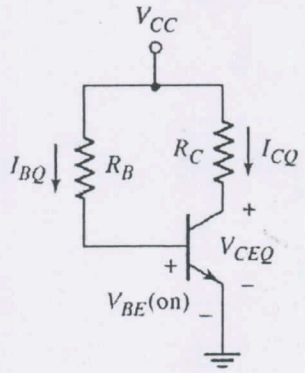
Department of ECE
III Semester
EC23C02 & ANALOG CIRCUITS DESIGN
(Regulation 2023)

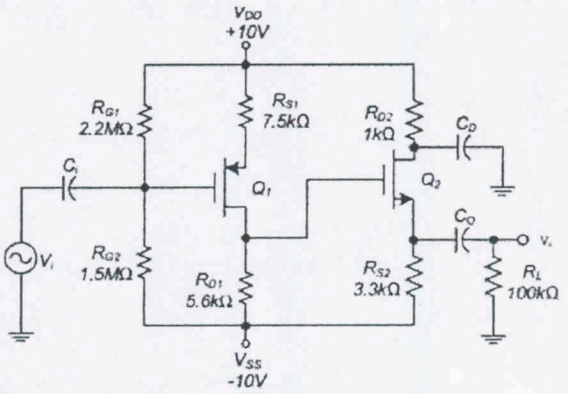
Time:3hrs Max.Marks: 100

CO1	Choose appropriate biasing circuits for BJT and MOSFET discrete amplifiers
CO2	Design and analyze single stage and multistage BJT amplifiers
CO3	Analyze the characteristic of MOSFET amplifiers, the effect of source and load
CO4	Analyze the high frequency response of BJT and MOSFET amplifiers
CO5	Design and analyze IC MOSFET amplifiers

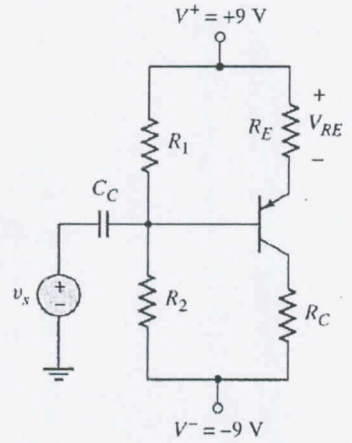
BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

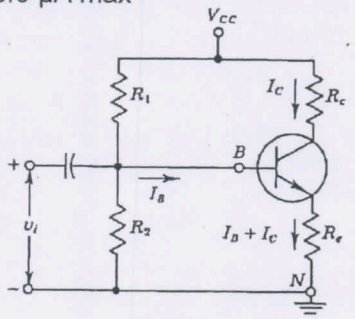
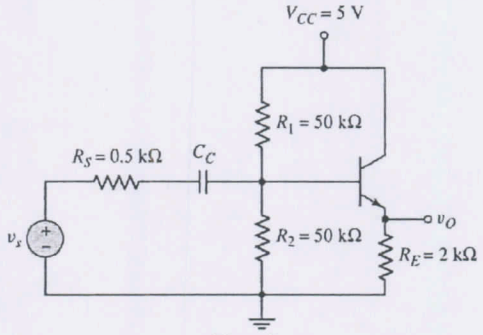
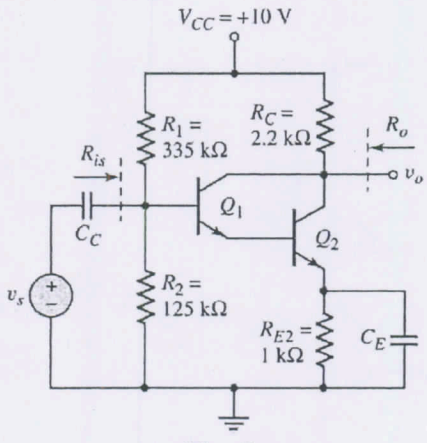
PART- A(10x2=20Marks)
(Answer all Questions)

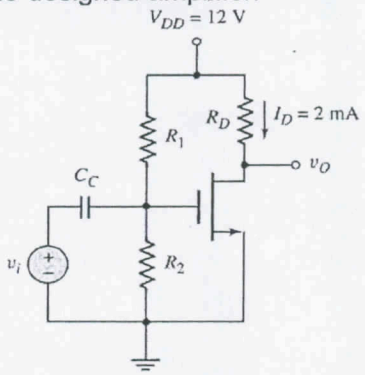
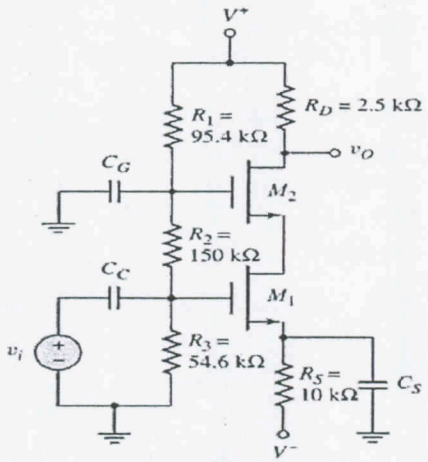
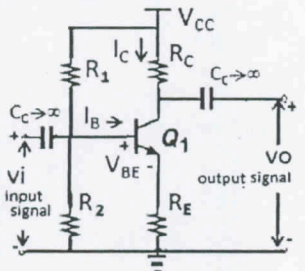
Q.No.	Questions	Marks	CO	BL
1	For the circuit shown in Fig. 1, the parameters are: $V_{EB(on)}$=0.6 V, and β=100. Find I_B, I_C, I_E such that V_{EC}=(1/2)V^+.  Fig. 1	2	1	L2
2	Sketch the DC load line for a BJT amplifier shown in Fig. 2 on the I_C–V_{CE} characteristic curves. Assume V_{CC} = 12 V, R_C = 6kΩ  Fig. 2	2	1	L2

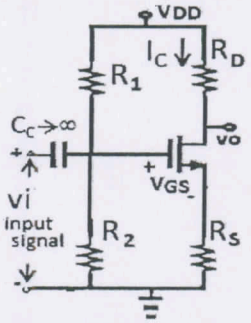
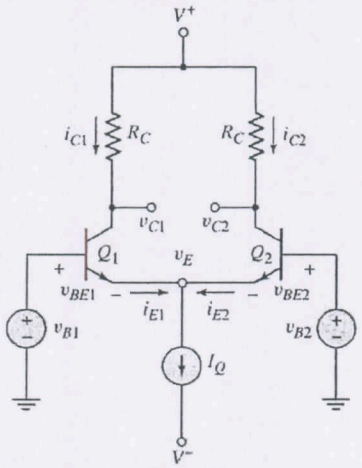
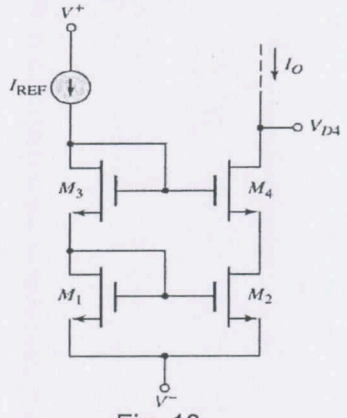
3	A common-emitter BJT amplifier has a V_{CC}=10 V and its quiescent operating point (Q-point) is set at V_{CEQ}=5 V. Assuming the output voltage swing is ideally limited by the distance to the saturation and cutoff regions, what is the maximum possible peak-to-peak output voltage swing?	**2**	2	L2
4	Two identical bipolar transistors, each with a current gain (β) of 50, are connected in a Darlington configuration. If the base current (I_B) entering the first transistor is 10μA, what is the approximate collector current of the second transistor?	**2**	2	L2
5	Draw the small signal ac equivalent circuit of the amplifier shown in Fig. 3  Fig. 3	**2**	3	L1
6	Calculate the drain current in an NMOS transistor with parameters V_{TN}=0.8 V, k'_n=80 μA/V², W=10μm, L=1.2 μm, and with applied voltages of V_{DS}=0.1 V and (a) V_{GS}=0 V, (b) V_{GS}=1 V.	**2**	3	L2
7	Describe the Miller effect and Miller capacitance.	**2**	4	L1
8	A bipolar transistor is biased at I_{CQ}=1 mA and has parameters C_π =10 pF, C_μ=2 pF, and β_o=120. Determine f_β.	**2**	4	L2
9	Sketch the Current steering circuit and explain the operation	**2**	5	L1
10	Define the common-mode rejection ratio, CMRR. What is the ideal value?	**2**	5	L1

PART- B(5x 13=65Marks)

Q.No.	Questions	Marks	CO	BL
11 (a)	Design a bias-stable pnp transistor circuit shown in Fig. 4. The transistor Q-point values are to be: V_{ECQ}=7 V, I_{CQ}≈0.5 mA, and V_{RE}≈1 V. Assume transistor parameters of β=80 and $V_{EB(on)}$=0.7 V.  Fig. 4	13	1	L4
	OR			

11 (b)	Design the self-bias circuit of Fig. 5 using a Si transistor type 2N3565 to meet the following specifications over the temperature range 25 to 65°C: $\Delta I_C/I_C \leq 15$ percent, V_{BE} at 25°C = 650 ± 50 mV, V_{CC}=20 V, β spread 150 to 600 at I_C = 1 mA and T=25°C, Lowest β at 25°C=150, highest β at 65°C=1,200, I_{CO} at 25°C = 50 nA max and I_{CO} at 65°C = 3.0 μA max  Fig. 5	13	1	L4
12 (a)	i) Derive the small signal voltage gain, input, and output resistance of the emitter-follower circuit shown in Fig. 6.  Fig. 6 ii) Calculate the input and output resistance of the circuit shown in Fig. 6. Assume R_s=0, and the transistor parameters are: β=100, $V_{BE(on)}$=0.7 V, and V_A=80 V.	8+5	CO2	L3
	OR			
12 (b)	i) Draw the small signal equivalent circuit for the amplifier shown in Fig. 7. Derive the expression for the overall small signal current gain β and input resistance Ris.  Fig. 7 ii) Assume the parameters of each transistor in Fig. 7 are β=100 and V_A = ∞. Determine the input and output resistances, Ris and Ro.	8+5	CO2	L3

13 (a)	Design the bias resistors (R_1, R_2) and the drain resistor (R_D) for the common-source NMOS amplifier circuit shown in Fig. 8 such that the Q-point is I_{DQ}=2 mA and located in the middle of the saturation region. Given V_{DD}=12 V and the constraint R1||R2 =100 kΩ, and using a transistor with V_{TN}=1 V, $k_{n'}$=80μA/V^2, W/L =25, and λ=0.015 V^{-1}, also determine the resulting small-signal voltage gain of the designed amplifier.  Fig. 8	13	CO3	L4
	OR			
13 (b)	The supply voltages to the cascode circuit in Fig. 9 are V$^+$=10 V and V$^-$=−10 V. The transistor parameters are: K_{n1}=K_{n2}=4 mA/V^2, V_{TN1}=V_{TN2}=1.5 V, and λ_1=λ_2=0. Let R_S=2 kΩ, and assume the current in the bias resistors is 0.1 mA. (a) Design the circuit such that I_{DQ}=5 mA and V_{DSQ1}=V_{DSQ2}=3.5 V. (b) Determine the resulting small-signal voltage gain.  Fig. 9	13	CO3	L4
14 (a)	Derive the expression for the short-circuit current gain of the BJT in the circuit shown in Fig. 10. Derive the alpha, beta cut-off frequency, and unity-gain bandwidth.  Fig. 10	13	CO4	L3
	OR			

14 (b)	Draw the high-frequency equivalent circuit for the CS amplifier circuit shown in Fig.11, and derive its voltage gain as a function of frequency. Derive its Miller capacitance and its upper corner frequency.  Fig. 11	13	CO4	L3
15 (a)	Draw the small signal equivalent circuit for the BJT differential pair shown in Fig. 12 and derive its differential-mode and common-mode gain and CMRR. Discuss the effect of a non-ideal current source (I_Q) with finite output impedance R_o on the CMRR.  Fig. 12	13	CO5	L3
	OR			
15 (b)	i) Draw a basic two-transistor NMOS current source and derive the output current in terms of reference current and aspect ratio of two transistors. ii) Derive the output resistance of the cascode configuration shown in Fig. 13 and show that it is much larger than that of the basic two-transistor current source.  Fig. 13	6+7	CO5	L3

PART- C(1x 15=15Marks)

Q.No.	Questions	Marks	CO	BL
16.	i) Design the circuit shown in Fig. 14 such that $v_o=v_{D1}-v_{D2}=1$ V when $v_1=-50$ mV and $v_2=+50$ mV. The transistor parameters are $V_{TN}=0.8$ V, $K_n=0.4$ mA/V^2, and $\lambda=0$.	8	3	L6

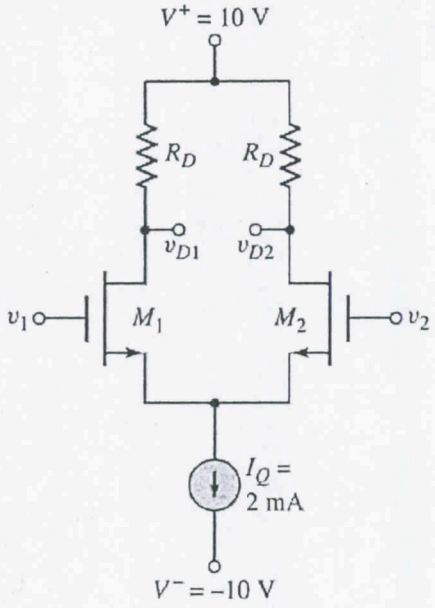


Fig. 14

	ii) The amplifier shown in the Figure 15 has parameters $V_{TN}=0.8$ V, $k'_n=100\mu A/V^2$, $W/L=50$, and $\lambda=0.02$ V^{-1}. The circuit parameters are $V^+=6$ V, $V^-=-6$ V, $I_Q=0.5$ mA, and $R_D=6$ kΩ. Evaluate the small-signal voltage gain for $R_L=10$ kΩ and determine the output resistance.	7	3	L5

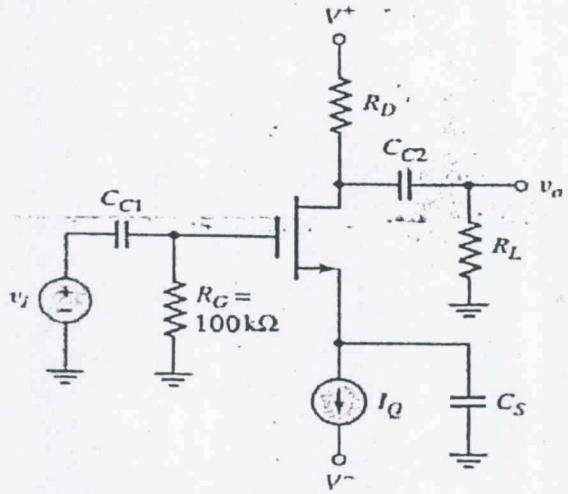


Fig. 15